HARPA

Harnessing Performance Variability

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HARPA Brochure

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Revisions List

Date	Version	Author(s)	Description
November 1, 2016	v0.1	Dimitrios Soudris	First Draft
November 15, 2016 2015	V0.2	HARPA partners	Revised version
November 30, 2016	v1.0	Dimitrios Soudris	Final Version

Executive Summary

This deliverable (due date M39) presents part of the results of the activity carried out in Task 6.1 (Dissemination) under the leadership of ICCS. The deliverable consists of the last version brochure of the HARPA project and it is derived from the press release appeared in the 50th issue of HiPEAC Newsletter.

The HARPA Brochure describes the main objectives, the technical approach of HARPA project and the Use Cases, will be regularly improved throughout the project and it available for download on the HARPA website.

EC FP7 STREP *HARPA* PROJECT:
Harnessing Performance Variability

FP7-ICT-2013-10-612069

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www.harpa-project.eu

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Politecnico di Milano (IT),
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ICCS/NTUA (GR)
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THALES (FR),
HENESIS (IT)

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Goal and Challenges

Continuously increasing application demands on both High Performance Computing (HPC) and Embedded Systems (ES) are driving the IC manufacturing industry on an everlasting scaling of devices in silicon. Nevertheless, integration and miniaturization of transistors comes with an important and non-negligible trade-off: time-zero and time-dependent performance variability. This article discusses key results of HARPA project, which aims to enable next-generation embedded and high-performance heterogeneous many-cores to cost-effectively confront variations by providing Dependable-Performance: correct functionality and timing guarantees throughout the expected lifetime of a platform under thermal, power, and energy constraints. The HARPA novelty is in seeking synergies in techniques that have been considered virtually exclusively in the ES or HPC domains (worst-case guaranteed partly proactive techniques in embedded, and dynamic best-effort reactive techniques in high-performance).

The HARPA team is composed of industry and academic partners across Europe specialized in fields covering all the abstraction layers, from hardware to application level. HARPA project has developed a set of monitors/knobs in hardware and software designs that observes the performance unpredictability, triggering system reactions. Figure 1 provides an overview of HARPA engine. It is a middleware split between the Operating System (HARPA-OS) and the hardware actuators (HARPA-RT) provides run-time dependable performance guarantees. HARPA-OS applies resource allocation policies, arbitrating the OS calls in a second time granularity. HARPA-RT sits at a low level in the system stack, achieving a millisecond control on hardware resources. HARPA-OS and HARPA-RT cooperate to ensure the performance dependability goals keeping a prompt low-level control on hardware resources. Run-time reactive and proactive techniques have been deployed, ensuring that the combined monitor/scheduling/knob reaction latency never violates the application deadlines. These techniques are tested on industrial applications running on embedded platforms and a full-system evaluation framework simulating HPC setups.

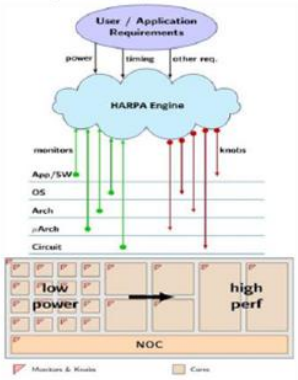

Fig.1(a): HARPA High-Level View

A fundamental objective of the project is to provide solutions to mitigate reliability threats and ensure dependable system performance. Towards this direction, the HARPA engine has been developed, implementing various control frameworks across the system stack. The goal is to exploit different manifestations of platform slack (i.e., slack in performance, power, energy, temperature, lifetime, and structures/components), in order to ascertain timing guarantees throughout the lifetime of the device. A component of the HARPA engine is the HARPA-OS, the system-wide resource manager developed by POLIMI. This component must include control policies capable of providing a response in a time frame spanning from hundreds of milliseconds to a second. The HARPA-RT sits at a low level in the system stack and is in direct contact with the various monitors and knobs. It has responsive control on hardware resources, enabling extremely fast adaptation to system behavior in the scale of some milliseconds, which is ideal for providing guarantees for hard-deadline applications and complements the comparatively slower responsiveness of the HARPA-OS.

The concepts that are to be developed within the HARPA context address equally both the HPC and ES domains. Specifically, from HPC domain we will use Disaster and Flood Management Simulation, while from ES domain Radio frequency spectrum sensing application, Face Detection Application, Object Recognition and Beesper Landslide Multimodal Monitoring. In particular, HARPA use cases will be demonstrated in HPC platforms: (i) Intel Xeon, (ii) x86-64 multi-core plus a GPU and Embedded platforms: (i) Freescale i.MX 6Quad, (ii) ODROID XU-3 (Octa Core Linux Computer Samsung Exynos5422 Cortex-A15 2.0Ghz quad core and Cortex-A7 quad core).

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